LIGHT EMITTING DEVICE AND MANUFACTURING METHOD OF THE SAME

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Cited documents:

- WO9946822
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Abstract of **WO2005101534**

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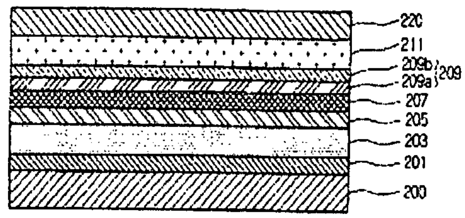

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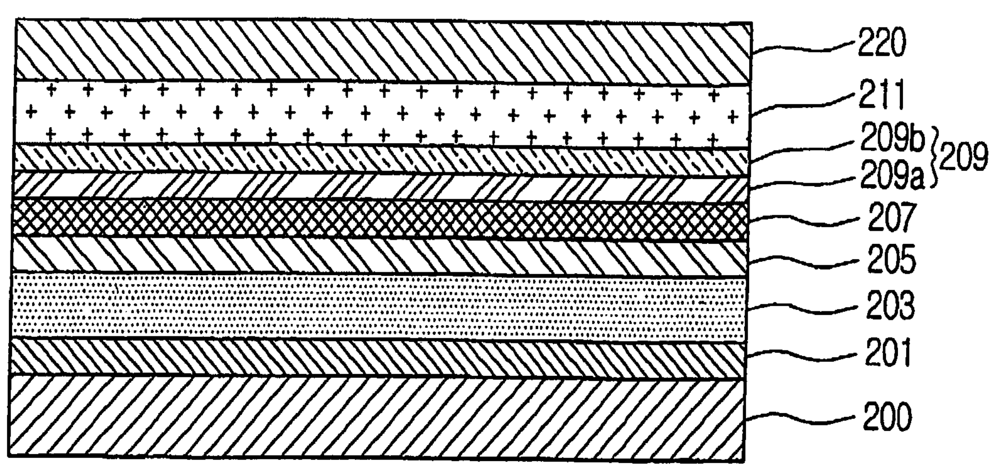
(54) Title: LIGHT EMITTING DEVICE AND MANUFACTURING METHOD OF THE SAME



(57) Abstract: A light emitting device is provided. In the light emitting device, a multi-layer for intercepting a reverse voltage applied to an active layer is formed between the active layer and a GaN layer. Accordingly, the reliability and operational characteristic of the light emitting device can be improved.

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LIGHT EMITTING DEVICE AND MANUFACTURING METHOD OF THE SAME

Technical Field

The present invention relates to a light emitting device, and particularly, to a light emitting device having an improved operational reliability and a manufacturing method of the same. More particularly, the present invention relates to a light emitting device providing an improved operational reliability by a structure in which it is protected from static electricity and its breakdown voltage is increased, and a manufacturing method of the same.

Background Art

A light emitting device is a kind of semiconductor device that converts electrical energy into light by using a characteristic of a compound semiconductor. The light emitting device is widely used for home appliances, a remote controller, an electronic display board, a display device, a variety of automation apparatuses, and the like. A typical example of the light emitting device is a light emitting diode (LED).

The LED is operated in such a way that electrons and holes are recombined with each other while moving through a PN-junction by a forward voltage applied to a semiconductor of a specific chemical element, and the fall of an energy level due to the electron-hole recombination causes light emission to occur.

The LED is generally manufactured to have a very small size of 0.25 mm^2 and is fixed using a mold. The LED has lead frames for applying a source voltage thereto and is mounted on a printed circuit board (PCB). A typical example of a LED package is a plastic LED package of 5mm (T 1 3/4), and a variety of LED packages are being developed in specific application fields. Meanwhile, with the trend of miniaturization and slimness of an information communication device, various components of the device such as a resistor,

a condenser and a noise filter are being further miniaturized. In accordance with this trend, the LED is also manufactured in the form of a surface mounted device (SMD) so as to be directly mounted on a PCB.

A color of light emitted from the LED is determined according to its wavelength obtained depending on a combination of elements constituting a semiconductor chip.

Recently, following red and green LEDs a blue LED has been developed, and the LED is being more widely used in various technical fields. For example, the LED is used as a white-light lamp or a light source for a display device. Moreover, the LED is further improved in its light luminance and thus is also used for an electronic display board and a camera of a mobile phone.

A general blue LED is constructed to include a sapphire substrate, a buffer layer formed on the sapphire substrate, an undoped GaN layer formed on the buffer layer, an N-type GaN layer formed on the undoped GaN layer, an active layer formed on the N-type GaN layer, and a P-type GaN layer formed on the active layer.

The active layer is a semiconductor layer made of luminescent material such as InGaN, and serves as a light-emitting region.

The P-type GaN layer is in contrast with the N-type GaN layer. When an external voltage is applied to the LED, electrons move from the N-type GaN layer into the active layer and holes move from the P-type GaN layer into the active layer. The electrons and the holes are then recombined with each other in the active layer to thereby cause light emission.

The abovementioned light emitting device has a drawback in that its reliability is degraded when its light luminance is improved, and vice versa. The light emitting device must have a high reliability so as to be used for a high-luminance electronic display board and a mobile phone. In order to improve the reliability of the light emitting device, each

layer formed in the device must be improved in crystallinity. However, the light emitting device has limitations in reliability improvement because it has structural limitations for emitting light of a desired wavelength.

Also, when a high voltage is applied to the light emitting device so as to improve its light luminance, its active layer is frequently damaged by the applied high voltage, causing the further degradation of its reliability.

Furthermore, when an electrostatic discharge (ESD) generated from electronic components near the light emitting device or from a human body is applied to the light emitting device, the light emitting device (specifically, its active layer) is frequently damaged by the applied ESD. To solve this problem caused by the ESD, an additional diode such as a Zener diode may be provided at a power input terminal of the light emitting device. However, this additional diode undesirably causes an increase in the manufacturing cost of the light emitting device.

Disclosure

Technical Problem

Accordingly, the present invention is directed to a light emitting device and a manufacturing method thereof that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a light emitting device having an improved operational reliability and a manufacturing method thereof.

Another object of the present invention is to provide a light emitting device having an improved light luminance without degradation in its reliability and a manufacturing method thereof.

A further object of the present invention is to provide a light emitting device that can be simply mounted on a desired apparatus because a separate diode need not be provided at its power input terminal and a manufacturing

method thereof.

Technical Solution

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, a light emitting device includes: a substrate; a gallium nitride layer provided above the substrate; an N-type gallium nitride layer provided above the gallium nitride layer; at least one $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer ($0<x,y<1$) provided above the N-type gallium nitride layer, x being different from y; and a P-type gallium nitride layer provided above the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer.

In another aspect of the present invention, a light emitting device includes: a first gallium nitride layer; a second gallium nitride layer; an active layer formed between the first gallium nitride layer and the second gallium nitride layer; and a multi-layer formed between the second gallium nitride layer and the active layer to intercept an applied electrostatic discharge.

In a further aspect of the present invention, a method for manufacturing a light emitting device includes the steps of: forming a buffer layer above a substrate; forming an N-type gallium nitride layer above the buffer layer; forming a multi-layer above the N-type gallium nitride layer, the multi-layer including layers of different growth temperatures; forming an active layer above the multi-layer; and forming a P-type gallium nitride layer above the active layer.

Advantageous Effects

The present invention makes it possible to improve the breakdown voltage characteristic and reliability of a light emitting device.

Also, the present invention makes it possible to protect a light emitting device (specifically, its active layer) from an electrostatic discharge and a high voltage

applied thereto.

Furthermore, the present invention makes it possible to improve the operational reliability of a light emitting device without degradation in the light efficiency thereof.

Moreover, the present invention makes it possible to reduce the manufacturing cost and volume of a light emitting device package because a separate diode for intercepting an applied ESD need not be provided at a power input terminal of the light emitting device.

Description of Drawings

FIGs 1 to 4 are sectional views illustrating a method for manufacturing a light emitting device according to an embodiment of the present invention.

FIG. 5 is a sectional view of a light emitting device according to an embodiment of the present invention.

FIG. 6 is an AFM image of a related art N-type GaN layer.

FIG. 7 is an AFM image of a multi-layer according to the present invention.

Best Mode for Carrying out the Invention

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIGs. 1 to 4 are sectional views illustrating a method for manufacturing a light emitting device according to an embodiment of the present invention, and FIG. 5 is a sectional view of a light emitting device according to an embodiment of the present invention.

The inventive manufacturing method for the light emitting device will now be described with reference to FIGs. 1 to 5.

Referring first to FIGs. 1 and 2, a GaN buffer layer 201 is formed on a sapphire substrate 200 at a predetermined temperature and then a slow-growth GaN layer 203 is formed on

the buffer layer 201. Here, the buffer layer 201 may be grown at 500~600 °C.

The GaN layer 203 is formed to prevent the defects of the buffer layer 201 from being transmitted to an undoped GaN layer (see 205 of FIG. 3) that is to be formed on the GaN layer 203 and to a nitride layer near the undoped GaN layer 205.

Referring to FIG. 3, the undoped GaN 205 is grown on the GaN layer 203 at a predetermined temperature and then a doped N-type GaN layer 207 is formed on the undoped GaN layer 205. Here, the undoped GaN layer 205 may be grown at 1000~1100 °C.

Referring to FIG. 4, an InGaN/InGaN multi-layer 209 for protecting the light emitting device from an ESD to thereby improve the operational reliability of the device is formed on the doped N-type GaN layer 207 prior to forming an active layer (see 211 of FIG. 5).

The InGaN/InGaN multi-layer 209 is constructed to include a first InGaN layer 209a formed on the doped N-type GaN layer 207 at a high temperature, and a second InGaN layer 209b formed on the first InGaN layer 209a at a low temperature. The first InGaN layer 209a may be grown to a thickness of 1~3000 Å at about 900 °C, and the second InGaN layer 209b may be grown to a thickness of 1~3000 at about 800 °C. Here, it should be apparent to those skilled in the art that the first and second InGaN layers 209a and 209b each may be grown in plurality. Also, the second InGaN layer 209b may be first formed on the doped N-type GaN layer 207 and then the first InGaN layer 209a may be formed on the second InGaN layer 209b.

In addition, the InGaN/InGaN multi-layer 209 may be formed to have a super lattice structure.

A method for forming the InGaN/InGaN multi-layer 209 will now be described in detail.

The InGaN/InGaN multi-layer 209 is grown using an alkyl source including TMGa and TMIn and a hydride gas including

NH_3 and N_2. Here, TMGa is 50~500 μ mol, TMIn is 25~500 μ mol, NH_3 and N_2 are 1~100 liter.

Also, the InGaN/InGaN multi-layer 209 is grown with H_2 being removed. Accordingly, H_2 is not included in the InGaN/InGaN multi-layer 209.

The first and second InGaN layers 209a and 209b have different In-Ga ratios because they are grown at different temperatures. A layer contains less In when it is grown at a higher temperature. Accordingly, the first InGaN layer 209a contains less In than the second InGaN layer 209b.

In content of the layers 209a and 209b can be expressed as Equation (1) below.

$$2\%(\text{1st InGaN layer}) \leq \frac{In}{InGa} \leq 3\%(\text{2nd InGaN layer}) \quad (1)$$

As seen from Equation (1), the second InGaN layer 209b grown at a lower temperature has more In content while the first InGaN layer 209b grown at a higher temperature has less In content.

The InGaN/InGaN multi-layer 209 has a plurality of hexagonal pits (see 10 of FIG. 7) formed thereon due to dislocation and defects resulting from the doped N-type GaN layer 207 and defects resulting from the super lattice structure.

The number of the hexagonal pits 10 is preferably 50 or less per area of 5μm×5μm.

The hexagonal pits 10 primarily reduce a current when a reverse voltage is applied to the light emitting device, and thus protects the active layer 211 from a high voltage applied thereto. Also, the hexagonal pits 10 can provide a bypath through which a current flows, thereby preventing the current from flowing through the active layer 211.

The hexagonal pits 10 serves as a kind of capacitor. That is, the capacitor (the hexagonal pits 10) is charged with a forward voltage when a forward voltage is applied to the light emitting device, and is charged with a reverse voltage when a reverse voltage due to an ESD is instantaneously applied thereto. Accordingly, a high ESD can

be prevented from being applied to the active layer 211. Consequently, the light emitting device can be protected from an externally-applied high voltage.

Referring to FIG. 5, the active layer 211 having an InGaN/InGaN structure of a multi-quantum well structure is grown on the InGaN/InGaN multi-layer 209. The active layer may be grown at about 600~800 °C. Finally, a P-type GaN layer 220 doped with impurities of Mg is grown on the active layer 211.

FIG. 6 is an AFM image of a related art N-type GaN layer, and FIG. 7 is an AFM image of a multi-layer according to the present invention.

Referring to FIGs. 6 and 7, while no pit is formed on a related art N-type GaN layer, a plurality of hexagonal pits 10 are formed on the InGaN/InGaN multi-layer 209.

The hexagonal pits 10 serve to remove a reverse current applied to the light emitting device or to provide a bypath through which a current flows, thereby preventing the active layer 211 being damaged by an externally-applied ESD. Consequently, the light emitting device can be protected from an externally-applied high voltage.

Table 1 below compares an anti-ESD durability of the inventive light emitting device with that of the related art light emitting device.

Table 1

Sample	Related art Light emitting device (volt)	Inventive light emitting device (volt)
1	-100	-2500
2	-100	-3000
3	-400	-4000
4	-300	-5000
5	-200	-5000

It can be seen from Table 1 that the inventive light emitting device equipped with the InGaN/InGaN multi-layer 209 can normally operate even when an about-20-time higher revere

voltage is applied thereto.

As described above, the present invention increases a breakdown voltage of the light emitting device and thus prevents an externally-applied ESD from affecting the light emitting device. Also, the present invention can provide a high breakdown voltage of the light emitting device by merely forming the InGaN/InGaN multi-layer 209 in the device.

Moreover, the photoluminescence characteristic of the InGaN/InGaN multi-layer 209 is maintained at a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below, whereby the operational reliability of the light emitting device can be further improved.

Mode for invention

While the present invention has been described and illustrated herein with reference to the preferred embodiments thereof, it will be apparent to those skilled in the art that various modifications and variations can be made therein without departing from the spirit and scope of the invention. For example, the inventive InGaN/InGaN multi-layer 209 may be used for a laser diode as well as a light emitting diode. Thus, it is intended that the present invention covers the modifications and variations of this invention that come within the scope of the appended claims and their equivalents.

Industrial Applicability

The present invention can improve an anti-ESD durability of a light emitting device while maintaining the light efficiency of the device.

Also, the present invention can improve the operational reliability of a light emitting device while maintaining the light efficiency of the device. Furthermore, the inventive light emitting device can stably operate even when a high voltage is applied thereto so as to increase its light luminance.

Moreover, the present invention can reduce the manufacturing cost of a light emitting device package because a separate diode for intercepting an applied ESD need not be provided at a power input terminal of the light emitting device.

Claims

1. A light emitting device comprising:

a substrate;

a gallium nitride layer provided above the substrate;

an N-type gallium nitride layer provided above the gallium nitride layer;

at least one $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer $(0<x,y<1)$ provided above the N-type gallium nitride layer, x being different from y; and

a P-type gallium nitride layer provided above the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer.

2. The device according to claim 1, wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a plurality of pits formed thereon.

3. The device according to claim 2, wherein the number of the pits is 50 or less per area of $5\mu m \times 5\mu m$.

4. The device according to claim 1, wherein each layer of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a thickness of 1~3000 Å.

5. The device according to claim 1, wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below.

6. A light emitting device comprising:

a first gallium nitride layer;

a second gallium nitride layer;

an active layer formed between the first gallium nitride layer and the second gallium nitride layer; and

a multi-layer formed between the second gallium nitride layer and the active layer to intercept an applied

electrostatic discharge.

7. The device according to claim 6, wherein the multi-layer is an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer ($0<x,y<1$).

8. The device according to claim 6, wherein the multi-layer has a plurality of pits formed thereon.

9. The device according to claim 6, wherein the multi-layer has a plurality of layers of different In content, the plurality of layers being alternately stacked in the multi-layer.

10. The device according to claim 6, wherein the multi-layer has a plurality of layers of different growth temperatures, the plurality of layers being alternately stacked in the multi-layer.

11. The device according to claim 6, wherein the multi-layer has two layers of different growth temperatures, the two layers being formed at 800°C and 900°C, respectively.

12. The device according to claim 6, wherein the multi-layer has a plurality of pits formed thereon, the number of the pits being 50 or less per area of $5\mu m \times 5\mu m$.

13. The device according to claim 6, wherein the multi-layer has a plurality of hexagonal pits formed thereon.

14. The device according to claim 6, wherein each layer of the multi-layer has In content of 3% or less with respect to Ga and In content.

15. The device according to claim 6, wherein each layer of the multi-layer has In content of 2% or less with respect to Ga and In content.

16. The device according to claim 6, wherein the second gallium nitride layer is an N-type GaN layer.

17. A method for manufacturing a light emitting device, the method comprising the steps of:

forming a buffer layer above a substrate;

forming an N-type gallium nitride layer above the buffer layer;

forming a multi-layer above the N-type gallium nitride layer, the multi-layer including layers of different growth temperatures;

forming an active layer above the multi-layer; and

forming a P-type gallium nitride layer above the active layer.

18. The method according to claim 17, wherein the multi-layer has a plurality of InGaN layers of different In content, the InGaN layers being alternately stacked in the multi-layer.

19. The method according to claim 17, wherein the multi-layer has a plurality of layers of different growth temperatures formed thereon, the different growth temperatures being a high temperature and a low temperature, respectively.

20. The method according to claim 19, wherein the high temperature is 900°C .

21. The method according to claim 19, wherein the low temperature is 800°C .

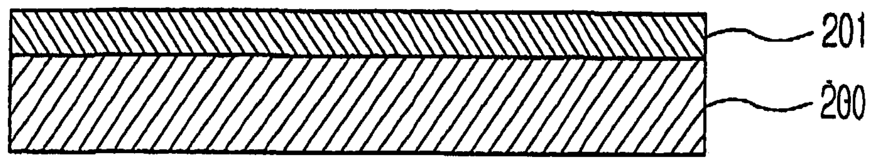
22. The method according to claim 17, wherein the multi-layer is formed using TMGa, TMIn, ammonium, and nitrogen.

23. The method according to claim 17, wherein each layer of the multi-layer has a thickness of 1~3000 Å.

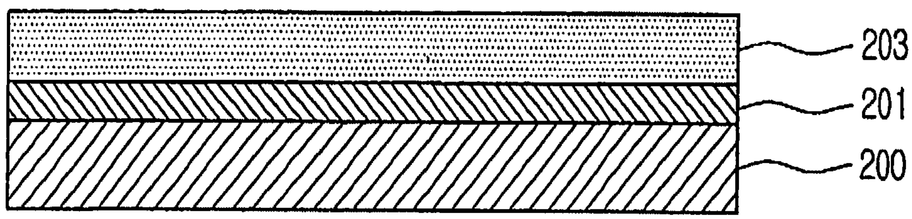
24. The method according to claim 17, further comprising the step of forming a slow-growth gallium nitride layer above the buffer layer.

25. The method according to claim 24, further comprising the step of forming an undoped gallium nitride layer above the slow-growth gallium nitride layer.

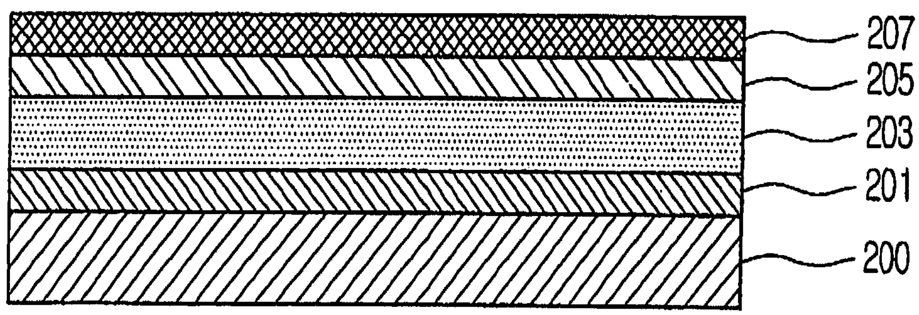
[Fig. 1]



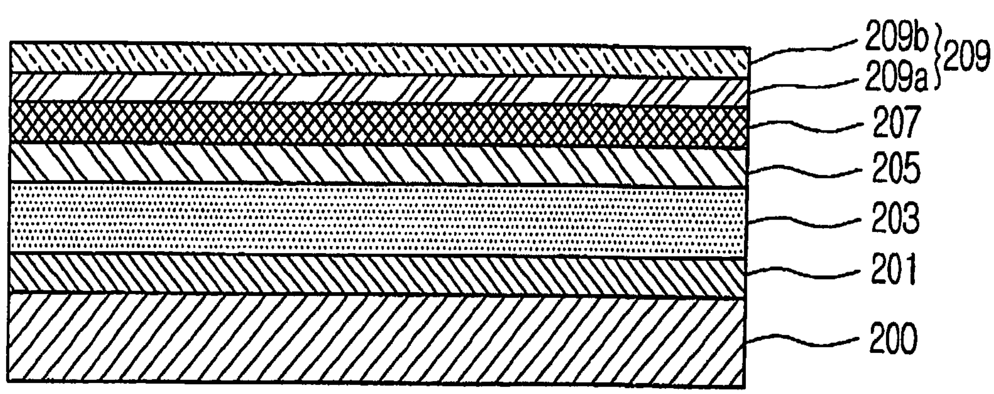
[Fig. 2]



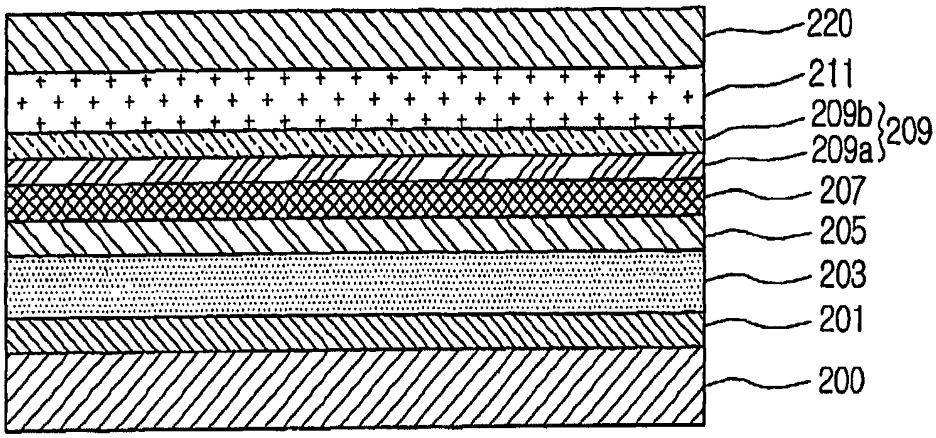
[Fig. 3]



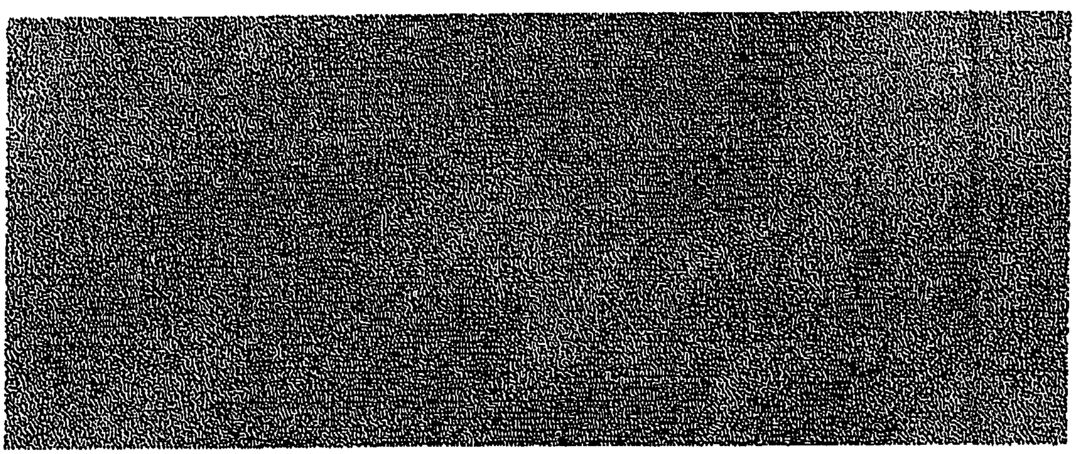
[Fig. 4]



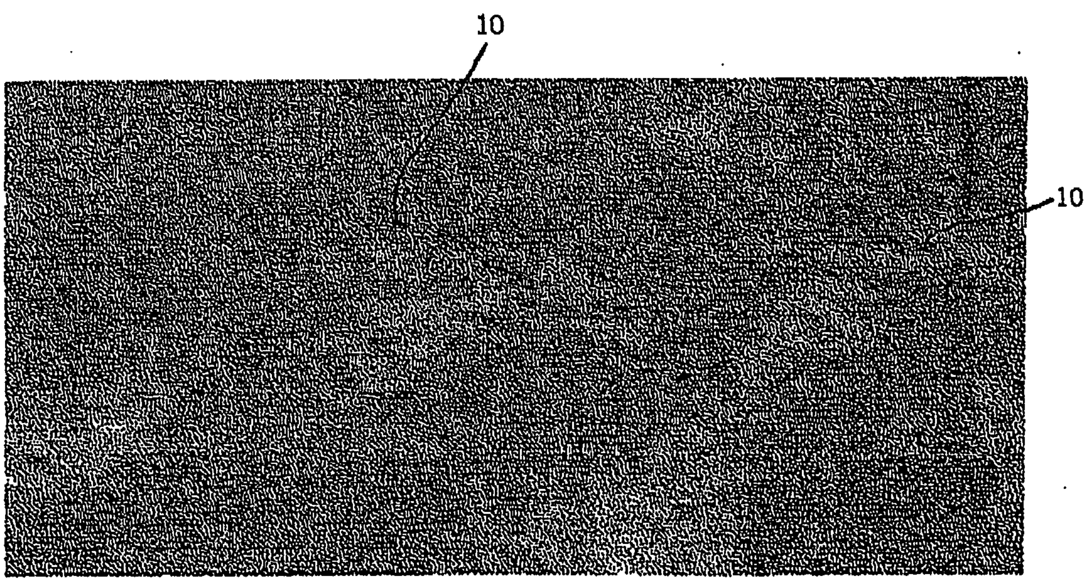
[Fig. 5]



[Fig. 6]



[Fig. 7]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/001045

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01L 33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Patents and applications for inventions since 1975
Korean Utility models and applictions for Utility models since 1975
Japanese Utility models and application for Utility models since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)
e-KIPASS : "electrostatic", "superlattice", "InGaN"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	WO 99/46822 A1 (NICHIA CHEM. IND. LTD.) 16 SEPTEMBER 1999 see the abstract, embodiments 1, 12, claims 1-2	1, 4, 6-7, 9 17-18; 22-23 2-3,5,8,10-16,19-21, 24-25
A	JP 11-220169 A (TOYODA GOSEI CO. LTD.) 10 AUGUST 1999 see the absttrract, figure 1	1-25
A	JP 2001-148507 A (NICHIA CHEM. IND. LTD.) 29 MAY 2001 see the abstract, full text, figure 1	1-25
A	JP 9-92880 A (TOYODA GOSEI CO. LTD.) 4 APRIL 1997 see the abstract, paragraph [0007], figure 1	1-25
A	JP 2001-298215 A (NICHIA CHEM. IND. LTD.) 26 OCTOBER 2001 see the abstract, figure 1	1-25
T	KR 10-448351 B (EPIVALLEY CO. LTD.) 2 SEPTEMBER 2004 see the abstract, figure 4	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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12 AUGUST 2005 (12.08.2005)	**12 AUGUST 2005 (12.08.2005)**

Name and mailing address of the ISA/KR	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2005/001045

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